What is Claimed is:

1. A NAND-type magnetoresistive RAM, comprising:

a plurality of transistors having gates to be connected one-by-one to a plurality of read wordlines and being connected in series as a NAND-type;

a bitline connected to a terminal transistor of the plurality of transistors connected in series at a read node; and

a plurality of MTJ cells each of which being connected to a connection node of two adjacent transistors, and each of which being controlled by a corresponding write wordline.

2. The NAND-type magnetoresistive RAM of claim 1, further comprising a register for temporarily storing data sequentially read from the plurality of MTJ cells in a read mode.

3. The NAND-type magnetoresistive RAM of claim 2, further comprising a controller for erasing data sequentially read from the plurality of MTJ cells in the read mode, and for sequentially restoring data stored in the register into the plurality of MTJ cells at the end of

the read mode.

4. The NAND-type magnetoresistive RAM of claim 3, wherein the controller reads and maintains data stored in the final MTJ cell of the plurality of MTJ cells.

5. The NAND-type magnetoresistive RAM of claim 3, wherein the controller controls the read wordlines to be sequentially enabled, from the read wordline connected to a gate of a transistor nearest to the read node, and to be maintained at an enable state until a final transistor is turned on.

6. The NAND-type magnetoresistive RAM of claim 3, wherein the controller controls write wordlines to be individually enabled in a write mode.

7. The NAND-type magnetoresistive RAM of claim 1, wherein other ends of the plurality of MTJ cells are connected to ground.

8. A NAND-type magnetoresistive RAM, comprising:

a plurality of transistors configured to be formed on a P-substrate, and configured to that a source and a drain

adjacent to the source share a common N-well region;

a plurality of read wordlines formed on gate regions of the plurality of transistors;

a plurality of MTJ cells each of which is connected to corresponding common N-well region;

a ground line formed in common on the plurality of MTJ cells;

a plurality of write wordlines being formed on the ground line, and corresponding to the plurality of MTJ cells respectively; and

a bitline configured to be connected to a terminal transistor of the plurality of transistors at a read, and formed on the plurality of write wordlines.

9. The NAND-type magnetoresistive RAM of claim 8, further comprising a plurality of contact regions for connecting the plurality of MTJ cells the common N-well regions .

10. The NAND-type magnetoresistive RAM of claim 8, further comprising:

a contact region formed on a source/drain region of the terminaltransistor and wherein the read node is formed on the contact region, and connected to the bitline.